ELECTRICALLY ALTERABLE NON-VOLATILE MEMORY
WITH N-BITS PER CELL

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of Application No.
10/428,732 filed May 5, 2003, which is a division of
Application No. 10/160,402 filed June 4, 2002, which is a
division of Application No. 09/794,041 filed February 28,
2001, which is a division of Application No. 09/493,138
filed January 28, 2000, which is a division of Application
No. 09/195,201 filed November 18, 1998, which is a division
of Application No. 08/911,731 filed August 15, 1997, which
is a division of Application No. 08/410,200 filed February
27, 1995, which is a division of Application No.
08/071,816, filed June 4, 1993, which is a continuation of
Application No. 07/652,878 filed February 8, 1991.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to non-volatile memory (NVM)
devices and, more particularly, is concerned with an
apparatus and method for programming and/or verifying
programming of a multi-level NVM device.

2. Description of the Background Art

In conventional single-bit per cell memory devices, the memory cell assumes one of two information storage states, either an "on" state or an "off" state. This combination of either "on" or "off" defines one bit of information. As a result, a memory device which can store n-bits of data requires n separate memory cells.

Increasing the number of bits which can be stored in a single-bit per cell memory device relies upon increasing the number of memory cells on a one-for-one basis with the number of bits of data to be stored. Methods for increasing the number of memory bits in a single memory device have relied upon the following advanced manufacturing techniques: manufacture larger die which contain more memory cells; or use improved lithography techniques to build smaller memory cells and allow more memory cells to be placed in a given area on a single chip.

An alternative approach to the single-bit per cell approach involves storing multiple-bits of data in a single memory cell. Previous approaches to implementing multiple-bit per cell non-volatile memory devices have only involved mask programmable read only memories (ROMs). In one of these approaches, the channel width and/or length of the

2

memory cell is varied such that 2^n different conductivity values are obtained which correspond to 2^n different states corresponding to n-bits of data which can be stored on a single memory cell. In another approach, the ion implant for the threshold voltage is varied such that the memory cell will have 2^n different voltage thresholds (Vt) corresponding to 2^n different conductance levels corresponding to 2^n different states corresponding to n-bits of data which can be stored on a single memory cell. Examples of memory devices of these types are described in U.S. Pat. No. 4,192,014 by Craycraft, U.S. Pat. No. 4,586,163 by Koike, U.S. Pat. No. 4,287,570 by Stark, U.S. Pat. No. 4,327,424 by Wu, and U.S. Pat. No. 4,847,808 by Kobatake.

Single-bit per cell read-only-memory devices are only required to sense, or read, two different levels or states per cell, consequently they have need for only one voltage reference. Sensing schemes for multi-level memory devices are more complex and require 2^n-1 voltage references. Examples of such multiple state sensing schemes for ROMs are described in U.S. Pat. No. 4,449,203 by Adlhoch, U.S. Pat. No. 4,495,602 by Shepard, U.S. Pat. No. 4,503,578 by Iwahashi, and U.S. Pat. No. 4,653,023 by Suzuki.

These approaches to a multi-bit ROM commonly have one of 2^n different conductivity levels of each memory cell being determined during the manufacturing process by means of a customized mask that is valid for only one data pattern. Thus, for storing n different data information patterns, a minimum of n different masks need to be produced and incorporated into a manufacturing process. Each time a data information pattern needs to be changed a new mask must be created and a new batch of semiconductor wafers processed. This dramatically increases the time between a data pattern change and the availability of a memory product programmed with that new data pattern.

Prior art electrically alterable multiple-bit per cell memory approaches store multiple levels of charge on a capacitive storage element, such as is found in a conventional dynamic random access memory (DRAM) or a charge coupled device (CCD). Such approaches are described in U.S. Pat. No. 4,139,910 by Anantha, U.S. Pat. No. 4,306,300 by Terman, U.S. Pat. No. 4,661,929 by Aoki, U.S. Pat. No. 4,709,350 by Nakagome, and U.S. Pat. No. 4,771,404 by Mano. All of these approaches use volatile storage, that is, the charge levels are not permanently stored. They provide 2^n different volatile charge levels on a

capacitor to define 2^n different states corresponding to n-bits of data per memory cell. All of these approaches have the common characteristic that whatever information is stored on such a memory cell is volatile because such a cell loses its data whenever power is removed. Furthermore, these types of memory cells must be periodically refreshed as they have a tendency to lose charge over time even when power is maintained.

It would be advantageous to develop a multi-bit semiconductor memory cell that has the non-volatile characteristic of a mask programmable read-only-memory (ROM) and the electrically alterable characteristic of a multi-bit per cell DRAM. These characteristics combined in a single cell would provide a multi-bit per cell electrically alterable non-volatile memory (EANVM) capable of storing K^n bits of data, where "K" is the base of the numbering system being used and "n" is the number of bits to be stored in each memory cell. Additionally, it would be advantageous if the EANVM described above was fully compatible with conventional industry standard device programmers/erasers and programming/erasing algorithms such that a user can program/erase the multi-bit per cell memory

5

in a manner identical to that used for current single-bit per cell memory devices.

SUMMARY OF THE INVENTION

The present invention provides a multi-level electrically alterable non-volatile-memory (EANVM) device, wherein some or all of the storage locations have more than two distinct states.

In a specific embodiment, the present invention provides a multi-level memory device. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in K^n memory states, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. The present multi-level memory device also includes a memory cell programming means for programming the multi-level cell means to a state corresponding to the input information. A comparator means for comparing, the memory state of the multi-level cell means with the input information is also included. The input information corresponds to one of a plurality of reference voltages. The present comparator

6

means further generates a control signal indicative of the memory state as compared to the input information.

An alternative specific embodiment also provides a multi-level memory devices. The present multi-level memory device includes a multi-level cell means for storing input information for an indefinite period of time as a discrete state of the multi-level cell means. The multi-level cell means stores information in K^n memory states, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$. A memory cell programming means for programming the multi-level cell means to a state corresponding to the input information is also included. The present multi-level memory device further includes a comparator means for comparing the memory state of the multi-level cell means with the input information. The input information corresponds to one of a plurality of reference voltages. The present comparator means further generates a control signal indicative of the memory state as compared to the input information. A reference voltage means for defining the plurality of reference voltages is also included. The present reference voltage means is operably coupled to the comparator means.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIG. 1 is a generic schematic representation of a non-volatile floating gate memory cell.

FIG. 2 is a block diagram of a prior art single-bit memory system.

FIG. 3 is a timing diagram of the voltage threshold of a prior art single-bit per cell EANVM system being programmed from an erased "1" state to a programmed "0".

FIG. 4 is a timing diagram of the bit line voltage of a prior single-bit per cell EANVM during a read operation. It illustrates waveform levels for both the programmed and erased conditions.

FIG. 5 is a block diagram of an M x N memory array implementing a multi-bit per cell EANVM system.

FIG. 6 is a block diagram for reading a multi-bit per cell EANVM system.

FIG. 7 shows the bit line voltage during a read cycle as a function of time for a 2-bit per cell EANVM which has

been programmed to one of four possible states, (0, 0), (1, 0), (0,1) and the fully erased condition (1,1). Four separate voltage levels are represented on this figure, each representing one of the four possible states. Only one of these would be present for any given read operation.

FIG. 8 is a block diagram of a multi-bit per cell system combining program/verify and read circuitry.

FIG. 9 is a timing diagram for the voltage threshold for a 2-bit per cell EANVM being programmed from a fully erased (1,1) state to one of the other three possible states.

FIG. 10 is a timing diagram which illustrates the voltage threshold of a 2-bit per cell EANVM being erased from a fully programmed (0,0) state to one of the other three possible states.

FIG. 11 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using fixed width program pulses.

FIG. 12 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses fixed width program pulses.

FIG. 13 is a timing diagram illustrating the voltage threshold of a 2-bit per cell EANVM during a program/verify cycle using variable width program pulses.

FIG. 14 is a timing diagram illustrating the bit line voltage of a 2-bit per cell EANVM during a program/verify process which uses variable width program pulses.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the specific embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the specific embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover various alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

In general, the invention described here allows n-bits of information to be stored on and read from an Electrically Alterable Non-Volatile Memory (EANVM). This is accomplished by electrically varying the conductivity of the channel of a floating gate FET to be within any one of

K^n conductivity ranges where "K" represents the base of the numbering system being employed (in a binary system, "K" equals 2). The conductivity range is then sensed and encoded. This forms the basis of an n-bit EANVM memory cell. The floating gate FET conductivity is electrically modified by using external programming hardware and algorithms which supply signals and voltages to the EANVM memory device.

These external signals and voltages are then modified internal to the device to provide an internally controlled program/verify cycle which incrementally stores electrons on the floating gate until the desired conductivity range is achieved. For the purpose of illustration, the n-bit per cell descriptions will assume a binary system which stores 2-bits per memory cell.

I. Prior Art Single-Bit EANVM Devices

FIG. 1 is a generic schematic representation of a non-volatile floating gate memory cell 10. It is not intended that this schematic drawing is in any way indicative of the device structure. It is used to illustrate the fact that this invention refers to an FET memory cell which uses an electrically isolated, or floating, gate 14 to store

11

charged particles for the purpose of altering the voltage

threshold and hence channel conductivity of the FET memory

cell 10.

The FET memory cell 10 includes a control gate 12

which is used either to select the memory cell for reading

or is used to cause electrons to be injected onto the

floating gate 14 during the programming process. Floating

gate 14 is an electrically isolated structure which can

indefinitely store electrons. The presence or absence of

electrons on floating gate 14 alters the voltage threshold

of the memory cell 10 and as a result alters the

conductivity of its channel region. A drain region 16 of

the FET is coupled to a source region 18 by a channel

region 19. When the floating gate 14 is fully erased and

the control gate 12 has been selected, the channel region

19 is in the fully "on", or high conductivity, state. When

the floating gate 14 is fully programmed the channel region

19 is in the fully "off", or low conductivity state.

FIG. 2 is a block diagram of a prior art conventional

single-bit EANVM memory system 30. The memory system 30

stores a single bit of information in an EANVM cell 32.

The cell 32, as described in FIG. 1, is selected for

reading or writing when a row, or word, select signal is

applied to a control gate terminal 34. A source terminal 36 for the FET of the cell 32 is connected to a reference ground potential. A drain terminal 38 is connected through a pull-up device 39 to a voltage Vpull-up at a terminal 40. Terminal 38 serves as the output terminal of the cell 32. When the cell 32 stores a "0" bit, the channel of the FET is in a low conductivity, or high impedance, state so that the voltage at terminal 38 is pulled-up to the voltage level Vpull-up on terminal 40. When the cell 32 stores a "1" bit, the channel of the FET is in a high conductivity, or low impedance, state so that the voltage at terminal 38 is pulled-down by the ground potential at terminal 36.

For reading the value of the single-bit stored in the cell 32, a sense amplifier 42 compares the voltage at terminal 38 with a reference voltage Vref at terminal 43. If a "0" is stored in the EANVM cell 32, the cell will be in a low conductivity state and as a result the voltage at terminal 38 is above the reference voltage at terminal 43. For a "0" stored in the cell 32, the output terminal 44 of the sense amplifier 42 will be a low voltage which will be transmitted through an output buffer 46 to a terminal 48 and then coupled to the I/O terminal 50 as a logical "0". If a "1" is stored on the EANVM cell 32, the cell is in a

high conductivity state and as a result the voltage at terminal 38 is below the reference voltage at terminal 43. The output of the sense amplifier 42 will be a high voltage which will be transmitted to the I/O terminal 50 as a logical "1".

For writing the value of an information bit stored in the cell 32, it is assumed that the cell 32 is in the erased, or fully "on", state which corresponds to a logical "1". The I/O terminal 50 is connected to the input terminal of an input latch/buffer 52. The output of the input latch/buffer 52 is connected to an enable/disable terminal 54 of a program voltage switch 56. The program voltage switch 56 provides a bit-line program voltage on a signal line 58 connected to terminal 38. Another output from the program voltage switch 56 is the word line program voltage on a signal line 62, which is connected to the control gate 34 of the EANVM cell 32. When a logical "0" is present at terminal 54 of the program voltage switch 56 from the output of Input Latch/Buffer 52 and when the program voltage switch 56 is activated by a program pulse on a signal line 62 from a program pulse 66, activated by a PGM/Write signal, the program voltage switch 56 provides the program voltage Vpp from a terminal 68 to the control

gate 34 of the EANVM cell 32. The program voltage switch

56 also biases the drain of the EANVM cell 32 to a voltage,

typically between 8 to 9 volts, and the gate of the EANVM

cell 32 to the program voltage Vpp, typically 12 volts.

Under these conditions, electrons are injected onto the

floating gate by a phenomenon known as hot electron

injection. This programming procedure raises the voltage

threshold of the EANVM cell which increases its source-

drain impedance. This continues until the FET memory cell

32 is effectively turned off, which corresponds to a "0"

state. When a "1" is present on terminal 54 from the

output of the Input Latch/Buffer 52 and when the PGM/Write

is enabled, the signal line 58 is driven low and

programming is inhibited and the "1", or erased, state is

maintained.

FIG. 3 is a timing diagram of a prior-art single-bit

EANVM cell 32, as described in connection with FIG. 2. The

timing diagram shows the change in voltage threshold of the

EANVM cell 32, as controlled by the word line and bit line

programming voltages, which are illustratively shown as a

single signal and which are both controlled by the

PGM/Write signal. The memory cell is being programmed from

the fully erased "1" state to the fully programmed "0"

state. For the duration of the PGM/Write pulse, the bit

and word line program voltages, which need not be the same,

are respectively applied to the drain connected to the bit

line terminal 38 and to the control gate 34 of the memory

cell 32. As electrons are injected onto the floating gate,

the voltage threshold of the memory cell begins to

increase. Once the voltage threshold has been increased

beyond a specific threshold value as indicated by the

dashed horizontal line, the memory cell 32 is programmed to

a "0" state.

Note that Fowler-Nordheim tunnelling can also be used

instead of hot electron injection to place electrons on the

floating gate. The multi-bit EANVM device described here

functions with either memory cell programming technique.

The prior art programming algorithms and circuits for

either type of programming are designed to program a

single-bit cell with as much margin as possible in as short

a time as possible. For a single-bit memory cell, margin

is defined as the additional voltage threshold needed to

insure that the programmed cell will retain its stored

value over time.

FIG. 4 is a timing diagram showing the bit line

voltage at terminal 38 as a function of time during a

memory read operation. In this example, prior to time t1 the bit line is charged to the Vpull-up condition. Note that it is also possible that the bit line may start at any other voltage level prier to time t1. At time t1 the EANVM cell 32 is selected and, if the cell 32 is in the erased or "1" state, the cell 32 provides a low impedance path to ground. As a result, the bit line is pulled down to near the ground potential provided at terminal 36 in FIG. 2. If the EANVM cell 32 were in the "0" or fully programmed state, the bit line voltage would remain at the Vpull-up voltage after time t1. The voltage on the bit-line terminal 38 and the reference voltage Vref at terminal 43 are compared by the comparator 42, whose buffered output drives I/O terminal 50. When Vref is greater than the bit line voltage, the output on I/O terminal 50 is a logical "1". When Vref is lower than the bit line voltage, the output on I/O terminal 50 is a logical "0".

II. Memory Array for a Multi-Bit EANVM System

FIG. 5 is a block diagram of a multi-bit per cell EANVM system 100 which includes an M x N array of memory cells. The cells are typically shown as a floating gate FET, or EANVM, 102, as described in connection with FIG. 1.

The array uses similar addressing techniques, external control signals, and I/O circuits as are used with currently available single bit per cell EANVM devices such as EPROM, EEPROM, FLASH, etc. devices. Row Address signals are provided at input terminals 103A and Column Address signals are provided at input terminals 103B.

Each of the EANVM cells in a row of cells has its source connected to a ground reference potential and its drain connected to a column bit line, typically shown as 106. Each of the columns is connected to a pull-up device, as indicated by the block 105. All of the control gates of a row are connected to a row select, or word, line, typically shown as 104. Rows are selected with a row select circuit 108 and columns are selected with a column select circuit 110. Sense amplifiers 112 are provided for each of the selected columns. Decode/encode circuits 114 and n-bit input/output latches/buffers 116 are also provided. A PGM/Write signal is provided at an input terminal 118 for activating a mode control circuit 120 and a timing circuit 122.

A significant feature of this n-bit per cell system 100 as compared to a single-bit per cell implementation is that the memory density is increased by a factor of n,

where n is the number of bits which can be stored on an individual multi-bit memory cell.

III. Basic Read Mode of an N-Bit Memory Cell

FIG. 6 shows a binary system 150 for reading the state of an n-bit floating gate memory cell 102, as described in connection with FIG. 1, according to the invention, where n is the number of bits stored in the memory cell. For this example, n is set to 2 and one of four states of the memory cell must be detected. The four possible states being, (0,0), (0,1), (1,0), or (1,1). Detecting which state is programmed requires a 3-level sense amplifier 152. This amplifier includes three sense amplifiers 154, 156, 158 each of which have their negative input terminals connected to the output terminal 168 of the memory cell 102. Sense amplifier 154 has a reference voltage Ref 3 connected to its positive input terminal. Sense amplifier 156 has a reference voltage Ref 2 connected to its positive input terminal. Sense amplifier 158 has a reference voltage Ref 1 connected to its positive input terminal. The voltage references are set such as follows: Vpull-up > Ref 3 > Ref 2 > Ref 1. The respective output signals S3, S2, S1 of the three sense amplifiers drive an encode logic circuit 160,

which encodes the sensed signals S3, S2, S1 into an
appropriate 2-bit data format. Bit 0 is provided at an I/O
terminal 162 and Bit 1 is provided at an I/O terminal 164.
A truth table for the encode logic circuit 160 is as
follows:

S3	S2	S1	I/O 1	I/O 0	State
L	L	L	0	0	(0,0)
H	L	L	1	0	(1,0)
H	H	L	0	1	(0,1)
H	H	H	1	1	(1,1)

During a read operation of an n-bit memory cell, the
levels of the respective output signals S3, S2, S1 of the
sense amplifiers 154, 156, 158 are determined by the
conductivity value to which the memory cell had been set
during a programming operation. A fully erased EANVM cell
102 will be in its lowest threshold voltage state, or the
highest conductivity state. Consequently, all of the
reference voltages will be higher than the bit line voltage
at terminal 168, resulting in a (1,1) state. A fully
programmed EANVM cell 102 will be in its highest threshold
voltage state, or its lowest conductivity state.

20

Consequently, all reference voltages will be lower than the bit line voltage at terminal 168, resulting in a (0,0) state. The intermediate threshold states are encoded as is illustrated in the truth table for the logic circuit 160.

FIG. 7 shows the bit line voltage as a function of time at terminal 168, during a read cycle, for a binary 2-bit per memory cell. For purposes of illustration, each of the four possible waveforms corresponding to the four possible programmed states of the memory cell are shown. During a read cycle only the waveform corresponding to the programmed state of the EANVM cell would occur. For example, assume the EANVM memory cell 102 has been programmed to a (1,0) state. Prior to time t1, because the EANVM cell 102 has not yet been selected or activated, the bit line 106 is pulled-up to Vpull-up. At time t1, the EANVM cell is selected using conventional memory address decoding techniques. Because the EANVM cell has been programmed to a specific conductivity level by the charge on the floating gate, the bit line is pulled down to a specific voltage level corresponding to the amount of current that the cell can sink at this specific conductivity level. When this point is reached at time t2 the bit line voltage stabilizes at a voltage level Vref3

between reference voltages Ref 3 and Ref 2 which correspond to a (1,0) state. When the EANVM cell 102 is de-selected, the bit line voltage will return to its pulled-up condition. Similarly, the bit-line voltage stabilizes at Vref2 the (0,1) state, or at zero volts for the (1,1) state.

FIG. 8 is a block diagram of an n-bit memory cell system 200. For purposes of illustration a binary 2-bit per cell system is shown. However, the concepts of the invention extend to systems where n is greater than 2. It is also intended that the invention include any system where the EANVM memory cell has more than two states. For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system. Some of the components of this system 200 are shown and described with the same reference numerals for the components of FIG. 6 for the read mode of operation. It is intended that these same reference numerals identify the same components.

The system 200 includes a memory cell 102, as described in FIG. 1, with a bit line output terminal 168. For the read mode of operation, a 3-level sense amplifier 152 with read reference voltages Ref 1, Ref 2, and Ref 3

and an encoder 160 is provided. Read data is provided at a Bit 0 I/O terminal 162 and at a Bit 1 I/O terminal 164. For the write mode of operation, a verify reference voltage select circuit 222 provides an analog voltage reference level signal X to one input terminal of an analog comparator 202. The verify reference voltages are chosen so that as soon as the bit line voltage on bit line 106 is greater than the verify reference voltage the threshold of the EANVM cell 102 is set to the proper threshold corresponding to the memory state to which it is to be programmed. To this end the verify reference voltages Vref1, Vref2, Vref3, and Vref4 are set such that Vref4 is above Ref 3, Vref3 is between Ref 3 and Ref 2, Vref2 is between Ref 1 and Ref 2, and Vref1 is below Ref 1. During a normal read operation, the bit line voltage will settle midway between the read reference voltages to insure that the memory contents will be read accurately. The verify reference voltage select circuit 222 is controlled by the 2-output bits from a 2-bit input latch/buffer circuit 224, which receives binary input bits from the I/O terminals 162 and 164. The Y signal input terminal of the analog comparator 202 is connected to the bit line output terminal 168 of the multi-level memory cell 102. The output signal

from the analog comparator is provided on a signal line 204 as an enable/disable signal for the program voltage switch 220. An output signal line 206 from the program voltage switch 220 provides the word line program voltage to the control gate of the EANVM cell 102. Another output signal line 106 constitutes the bit line and provides the bit-line programming voltage to the bit-line terminal 168 of EANVM cell 102. After a program/verify timing circuit 208 is enabled by a PGM/Write signal provided on a signal line 212 from a PGM/Write terminal 214, the timing circuit 208 provides a series of program/verify timing pulses to the program voltage switch 220 on a signal line 210. The pulse widths are set to control the programming process so that the voltage threshold of the EANVM cell 102 is incrementally altered by controlling the injection of charge onto the floating gate of the EANVM cell. Each programming cycle increases the voltage threshold and, as a result, decreases the conductance of the memory cell 102. After each internal program cycle is complete, as indicated by signal line 210 going "high", the program voltages are removed via the program voltage switch 220 and a verify cycle begins. The voltage threshold of memory cell 102 is then determined by using the comparator 202 to compare the

24

bit line voltage at terminal 168 with the selected verify

reference voltage from the verify reference voltage select

circuit 222. When the bit line voltage exceeds that

supplied by the verify reference voltage select circuit

222, the output signal 204 from the comparator 202 will

then disable the program voltage switch 220 ending the

programming cycle. For this embodiment of the invention,

during a write operation, comparison of the current memory

cell analog contents with the analog information to be

programmed on the memory cell 102 is performed by the

analog comparator 202. The verify reference voltage select

circuit 222 analog output voltage X is determined by

decoding the output of the n-bit input latch/buffer 224

(n=2 in the illustrative form). The Y input signal to the

analog comparator 202 is taken directly from the bit line

terminal 168. Note that the 3-level sense/encode circuits

152, 160, and reference voltage select circuit 222 may be

completely independent as indicated in the drawing.

Alternatively, they may be coupled together to alternately

time share common circuit components. This is possible

because the 3-level sense/encode circuits 152 and 160 are

used in the read mode of operation while the verify

reference voltage select circuit 222 is used only in the write/verify mode of operation.

IV.   Basic Write Mode for a Multi-Bit per Cell EANVM System

In the write mode, a binary n-bit per cell EANVM system must be capable of electrically programming a memory cell to 2^n uniquely different threshold levels. In the two-bit per cell implementation, because it is assumed that the cell starts from the erased (1,1) state, it is only necessary to program three different thresholds (Vt1, Vt2, and Vt3) which define the (0,1), (1,0), and (0,0) states. Vt1 is the threshold required such that in the read mode, the bit line voltage will fall between Ref 1 and Ref 2. Vt2 is the threshold required such that in the read mode, the bit line voltage will fall between Ref 2 and Ref 3. Vt3 is the threshold required such that in the read mode, the bit line voltage will be greater than Ref 3.

FIG. 9 illustrates the change in voltage threshold for a 4-level, or 2-bit EANVM cell as the floating gate is being charged from an erased (1,1) threshold state to any one of the three other possible states. In prior art single-bit memory cells where there are only two states, the design objective is to provide enough charge to the

floating gate to insure that the cell's voltage threshold is programmed as high as possible, as shown in FIG. 3. Because there is no upper threshold limit in a single-bit per cell system, overprogramming the cell will not cause incorrect data to be stored on the memory cell.

As will be appreciated from FIG. 9, in an n-bit per cell system the memory cell must be charged to a point so that the voltage threshold is within a specific voltage threshold range. In this example, where the cell is being programmed to a (1,0) state, the proper threshold range is defined as being above a threshold level Vt2 and as being below a threshold level Vt3.

To accomplish this n-level programming it is necessary to add to or modify the prior art EANVM circuitry. FIG. 8 shows the additional or modified circuits, including a reference voltage select, an n-bit latch/buffer, a program/verify timing circuit, and a comparator. The comparator can be either digital or analog.

FIG. 10 illustrates the voltage threshold of an EANVM cell as the floating gate is being erased from a (0,0) state. Standard EANVM programming operating procedure calls for a memory cell to be erased prior to being programmed. This erasure can be performed at the byte,

block, or chip level and can be performed by electrical, UV, or other means. In this type of system the cell would be completely erased to a (1,1) state prior to initiating a programming cycle. If a system has the capability to erase an individual memory cell, then it is not necessary to erase all of the cells of a group prior to initiating a programming operation. It is then possible to incrementally erase an individual memory cell, as necessary, to program the cell to the appropriate voltage threshold as is indicated by the waveforms labelled (1,0) and (0,1).

FIG. 11 is a timing diagram which illustrates how a 2-bit EANVM cell of FIG. 8 is programmed from an erased (1,1) state to a (1,0) state using the timing circuitry 208 to generate fixed length timing pulses. A low logic level state of the PGM/Write signal on signal line 212 enables the timing circuit 208. When enabled at time t1, the timing circuit 208 provides an internal fixed-width low level internal PGM timing pulse on signal line 210 to the program voltage switch 220. For the duration of the low state of the internal PGM timing pulse, the bit line and word line program voltage outputs on lines, 106 and 206 will be raised to their respective programming voltage

levels as shown in FIG. 11. During this programming

process, charge is added to the floating gate of the memory

cell 102. When the internal PGM timing pulse from timing

circuitry 208 switches to a high level, the programming

voltages are removed and a verify cycle begins. For this

example, verify reference voltage Vref3 is compared with

the bit line voltage. This internally controlled

program/verify cycle repeats itself until the bit line

voltage on terminal 168 exceeds Vref3. At this time, t2,

the EANVM cell 102 is verified to have been programmed to a

(1,0) state and programming is halted by the comparator 202

providing a disable signal on signal line 204 to the

program voltage switch 220.

FIG. 12 illustrates the bit line voltage of a 2-bit

per cell EANVM as it is being programmed from a fully

erased, or fully "on", state (1,1) to a partially "off"

state (1,0) using fixed length program pulses. When the

externally applied PGM/Write pulse is applied at time t1,

the program/verify timing circuit 208 first initiates a

verify cycle to determine the current status of the memory

cell 102. This is indicated by the bit line voltage being

pulled to a ground condition from, in this example, Vpull-

up. More generally, prior to time t1, the bit line voltage

could be pre-set to any voltage level. Once the cell has

been determined to be at a condition below the verify

reference voltage, Vref3 in this example, corresponding to

the data to be programmed, the first program cycle is

initiated. This is represented by the bit line voltage

being pulled up to Vprogram. After the first fixed length

programming pulse ends, a verify cycle begins. This is

represented by the bit line voltage being pulled down to a

point midway between ground potential and Ref 1. During

each successive verify cycle the bit line voltage is

observed to incrementally increase. This program/verify

cycle continues until the bit-line voltage exceeds the

selected verify reference voltage, in this case Vref3,

which indicates a memory state of (1,0), at time t2.

FIG. 13 illustrates how a 2-bit EANVM cell is

programmed from an erased (1,1) state to a (1,0) state

using variable length programming pulses. The internal PGM

pulses for this implementation start with a low state

longer than for fixed-width implementation of FIGS. 11 and

12. The low-state pulse widths grow progressively shorter

as the memory cell approaches the appropriate voltage

threshold. This approach requires more precise control

than the fixed length approach. However, programming times
can be greatly reduced on average.

FIG. 14 illustrates the bit line voltage of a 2-bit
per cell EANVM as it is being programmed from a fully
erased, or fully "on", state (1,1) to a partially "off"
state (1,0) using variable length program pulses. When the
externally applied PGM/Write pulse goes to an active low
level at time t1, the program/verify timing circuit 208
first initiates a verify cycle to determine the current
status of the memory cell 102. This is indicated by the
bit line voltage being pulled to a ground condition from,
in this example, Vpull-up. Although, prior to time t1, the
bit line voltage could be pre-set to any voltage level.
Once the cell has been determined to be at a condition
below the verify reference voltage corresponding to the
data to be programmed, Vref3 in this example, the first
program cycle is initiated. This is represented by the bit
line voltage being pulled up to Vprogram. After the first
variable length programming pulse is over, another verify
cycle begins. This is represented by the bit line voltage
being pulled down to a point midway between Ref 1 and Ref
2. During each successive verify cycle the bit line
voltage is observed to incrementally increase. This

program/verify cycle continues until the bit-line-voltage surpasses the selected verify reference voltage, in this case Vref3 which indicates a memory state of (1,0), at time t2.

Accordingly, the programming process for an n-bit per cell EANVM uses program/verify cycles, to incrementally program a cell. The durations of these cycles are determined by the timing circuit 208. A key element of the system is to provide a programming scheme which provides for accurate programming of the memory cell 102. This is accomplished by matching the pulse widths of the timing pulses of the timing circuitry 208 to the program time of the EANVM cell being used. As indicated in FIGS. 11 and 13, a desired voltage threshold actually falls within a range of threshold voltages. If the program pulses are too long, then too much charge may be added to the floating gate of the memory cell 102. This may result in an overshoot of the target voltage threshold, resulting in incorrect data being stored in the memory cell.

The programming pulse width is set such that if the voltage threshold of the cell 102 after the (n-1)th programming pulse is at a point just below the target voltage threshold, then the (n)th, or final, program pulse

will not cause an overshoot resulting in an overprogrammed condition for a memory cell.

FIG. 8 may also use a digital comparator rather than the analog comparator 202 shown in FIG. 8. The digital comparator would use the encoded data from the encode circuitry 160, which represents the current contents of the EANVM cell 102, as the input to the comparator. The verify reference voltage select 222 would provide the voltage to be encoded with the input coming from the output of the n-bit input latch/buffer 224, representing the data to be programmed. Otherwise, the function of the comparator within the system remains the same.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use

contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.